REMARKS AND ARGUMENTS

Allowed claims

The Examiner has allowed claims 13-16. These claims are patentable over the cited art of record.

Objection to the claims

Claims 2-12, 18-19, 21-22 and 24-25 are objected to by the Examiner as being depending upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. In particular, these claims contain subject mater which is not taught or suggested by the art of record. See Office Action mailed June 9, 2006, page 5.

Applicant, in response, has amended claim 2 and claim 18 to include the limitations of their respective base claims (1 and 17). Claim 19 has been amended to be dependent on claim 18. As for claim 20, Applicant has amended it to include the limitations of claim 21. Claim 21 has been cancelled in view of the amendments to claims 20. Applicant now submits that amended claims 2, 18 and 20 are now patentable. Since claims 3-12, 19 and 22-25 are directly or indirectly dependent on claim 2, 18 or claim 20, these claims are also patentable over the art of record.

Rejection under 35 USC §102

Claims 1, 20 and 23 are rejected under 35 USC § 102(b) as being anticipated by Sartore et al. (US Patent No. 5,887,272). Applicant submits that this basis of rejection for claims 20 and 23 is moot in view of the amendments to claim 20. As to claim 1, Applicant respectfully disagrees.

Claim 1, by way of this response, has been amended to more clearly recite the invention. As amended, claim 1 recites an IC comprising a memory cell array having a plurality of memory cells, wherein each memory cell includes at least a first port and at least a second port. The first and second ports of the memory cells form at least first and second access ports of the memory cell array for

accessing the memory cells. A cache memory is coupled to said first and second access ports, wherein during a read operation to the memory cell array to obtain read data through one of said first and second access ports, the cache memory provides the read data if the read data is contained therein or the memory cell array provides the read data if the read data is not contained in the cache memory. A refresh control circuit for performing refresh operations for said memory cells.

Sartore et al. (Sartore) describes a DRAM array containing embedded row registers that function as an on-chip cache. The subarray includes dedicated read and write ports. Sartore nowhere describes the use of memory cells having at least first and second ports. Although Sartore's cell array includes dedicated read and write ports, the array read and write ports are commonly coupled to the single port of the memory cell. With respect to the row registers, Sartore describes that in the event of a read miss, data read out of the memory is also loaded to the row registers. See Sartore, col. 6 at line 62 to col. 7 at line 3. Nowhere does Sartore teach or suggest coupling the row register to the write port. Sartore, at best, only teaches or suggests coupling the row register to only one port, not two access ports as claimed. Applicant therefore submits that claim 1, as amended, is patentable over Sartore and respectfully requests withdrawal of this basis of rejection.

As for claim 17, it is rejected under 35 USC § 102(e) as being anticipated by Rao (US Patent No. 6,256,256). Applicant respectfully disagrees.

Claim 17 has been amended to more clearly recite the invention. Claim 17, as amended, recites an IC comprising a memory cell array having a plurality of memory cells with at least first and second ports forming a memory cell array with at least first and second access ports. A cache memory is coupled to the first and second access ports, wherein the cache memory can be accessed through either of the access ports. The first and second access ports comprise address terminals and data terminals, the second access port being controlled by a refresh control circuit to perform a refresh of said memory cells.

Rao describes a multiport memory cell array having a pair of independent access ports, allowing two different external devices to access the array simultaneously. An access port is coupled to a CPU associated with an external (L2) cache. *See* Rao, Figs. 10A, 10B and 11. As shown, the

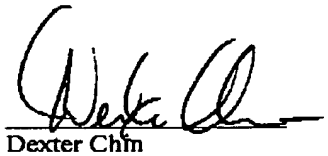
external cache is coupled to only one of the access ports. Even assuming that each access port was coupled to a separate CPU with its associated cache, each cache would still only be coupled to one, and not both, of the access ports. Therefore, Rao fails to teach or suggest providing a cache memory coupled to the first and second access ports, wherein the cache memory can be accessed through the access ports as required by claim 17. Applicant therefore submits that claim 17 is patentable over Rao.

Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance and the issuance of a formal Notice of Allowance at an early date is respectfully requested. Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

Date: September 11, 2006

Respectfully submitted,



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